REMARKS

Introduction

This Reply is in response to the Office Action of December 23, 2005. Reconsideration of this application in view of the following remarks is respectfully requested.

Claims 7-11, 13-16, 18 and 19

Claims 7-11, 13-16, 18, and 19 were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

This has been done by placing claims 7-11, 13-16, 18, and 19 into independent form. Claims 7-11 formerly depended on claim 1. The features of claim 1 have therefore been incorporated into amended claims 7-11. Claims 13-16, 18, and 19 formerly depended on claim 12, so the features of claim 12 have been incorporated into amended claims 13-16, 18, and 19.

In view of these amendments, claims 7-11, 13-16, 18, and 19 are in condition for allowance.

Claims 1-6, 12, and 17

Claims 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Goode U.S. patent 4,953,185. Claims 2-3, 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Goode in view of Garlepp et al. U.S. Patent

6,920,622. Claim 4 was rejected under 35 U.S.C. S103(a) as being unpatentable over Goode in view of Saito U.S. 2002/0145480. Claims 12 and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Goode in view of Doblar et al. U.S. Patent 6,516,422. These rejections are respectfully traversed.

Applicants' invention relates to clock and data recovery circuits with automatic mode switching. In a typical high-speed serial communications arrangement, a transmitter sends high-speed serial data to a receiver. The transmitter embeds a clock signal with the serial data. At the receiver, a clock and data recovery circuit is used to extract the embedded clock. Once the clock and data recovery circuit has recovered the clock signal from the incoming data stream, the data can be deserialized and distributed to circuitry on the receiving integrated circuit.

Independent claims 1 and 12 are directed to clock and data recovery circuits containing two phase-locked loops. A first of the two phase-locked loops locks onto a reference clock when the clock and data recovery circuit is operated in a reference mode. A second of the two phase-locked loops locks onto the incoming serial data stream when the clock and data recovery circuit is operated in a data mode. Operation of the clock and data recovery circuit is controlled automatically

using a control circuit. The control circuit automatically switches the clock and data recovery circuit between the reference mode (in which the first phase-locked loop is being used to lock onto the reference clock) and the data mode (in which the second phase-locked loop is being used to lock onto the incoming serial data stream).

An illustrative embodiment of applicants' clock and data recovery circuit is shown in FIG. 3 of applicants' specification. As shown in FIG. 3, the reference clock is applied to a reference clock input terminal 23. The serial data stream is applied to the serial data input 58 formed by the DATAP and DATAN lines. The first and second phase-locked loops each have a separate phase detectors, but share other components. The first phase-locked loop uses phase/frequency detector 60. The second phase-locked loop uses phase detector 88. The charge pump 66, loop filter 72, and voltage-controlled oscillator 78 are shared by the two phase-locked loops. A recovered clock signal is provided at the output of the voltage-controlled oscillator 78. This output is shared by the first and second phase-locked loops. As shown in FIG. 3, the recovered clock may be applied to circuitry such as deserializer 26 to use in processing recovered data on line 24.

Claims 1 and 12 have been amended to more clearly define how applicants' clock-and-data recovery circuit uses the

a parallel phase-locked-loop architecture with shared components of the type shown in FIG. 3. The clock-and-data recovery circuits of claims 1 and 12 each have two inputs and an output. A first of the clock-and-data recovery circuit inputs is a reference clock input. The signal from the reference clock input is processed by the first phase-locked loop. A second of the clock-and-data recovery circuit inputs is a serial data stream input. The signal from the serial data stream input is processed by the second phase-locked loop. The clock-and-data recovery circuit has a single recovered clock output, which is shared by the first and second phase-locked loops. When the first phase-locked loop is switched into use by the control circuit, the first phase-locked loop produces a reference clock signal on the recovered clock output. When the second phase-locked loop is switched into use by the control circuit, the second phase-locked loop produces a recovered clock signal on the same recovered clock output.

The prior art does not show or suggest the features of claims 1 and 12.

The Goode patent, which was said to anticipate claim 1 and which was used in combination with Doblar in rejecting claim 12, is directed towards a clock and data recovery circuit that uses a serial architecture based on discrete integrated circuits. In Goode's RX mode, received signals are processed by

squaring circuit 210, as shown in FIG. 2. The output of circuit 210 is provided to the input of phase-locked loop 230 through switch 220. The output of phase-locked loop 230 is provided to node 235. Phase-locked loop 250 is connected in series with phase-locked loop 230. As a result, phase-locked loop 250 receives the output of phase-locked loop 230 at its input 245 via switch 240. The clock output of the second phase-locked loop 250 is provided on output 125 of the clock recovery circuit.

Claims 1 and 12 require that the first and second phase-locked loops provide respective output signals directly to the same clock-and-data recovery circuit recovered clock output. In Goode's arrangement, the output of the phase-locked loop 230 is not connected at the clock output 125, but rather is connected to the input of phase-locked loop 250. Because of Goode's serial placement of phase-locked loops 230 and 250, Goode's arrangement does not allow the output of the phase-locked loop 230 to be supplied directly to the clock output 125 as required by claims 1 and 12.

The Doblar patent, which the Office Action relied upon as showing an override signal in connection with the rejection of claim 12, also fails to show or suggest any use of two phase-locked loops with a shared recovered clock output of the type defined in applicants' claims. The circuitry of the Goode

patent, whether taken alone or in combination with Doblar, therefore does not meet the limitations of claims 1 and 12. Claim 1, which was rejected as being anticipated by Goode and claim 12, which was rejected based on a proposed combination of Goode and Doblar, are therefore in condition for allowance. Claims 2-6 are allowable because they depend on allowable claim 1. Claim 17 is allowable because it depends on allowable claim 12.

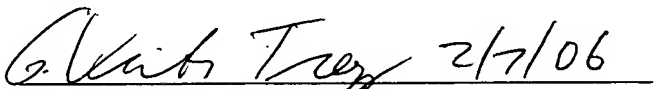
Claims 20-26

Claims 20-26 have been allowed.

Conclusion

The foregoing demonstrates that claims 1-26 are patentable. This application is therefore in condition for allowance. Reconsideration and allowance of the application are respectfully requested.

Respectfully submitted,



G. Victor Treyz
Reg. No. 36,294
Attorney for Applicants
Customer No. 45851